Subject Name:COMPUTER ORGANISATION & OPERATING SYSTEMS

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Year and Sem, Department: III/II ECE

Unit-I: (Title)

Important points / Definitions:

1A **Register** is a group of flip-flops with each flip-flop capable of storing **one bit** of information. An n-bit register has a group of n flip-flops and is capable of storing binary information of n-bits.

2. Information transferred from one register to another is designated in symbolic form by means of replacement operator.

R2 ← R1

It denotes the transfer of the data from register R1 into R2.

3. **Add Micro-Operation**

It is defined by the following statement:

```
R3 → R1 + R2
```

The above statement instructs the data or contents of register R1 to be added to data or content of register R2 and the sum should be transferred to register R3.

4. **Shift Micro-Operations**

These are used for serial transfer of data. That means we can shift the contents of the register to the left or right. In the **shift left** operation the serial input transfers a bit to the right most position and in **shift right** operation the serial input transfers a bit to the left most position.

5. **Addressing Modes** can be defined as-
"The technique for specifying the address of the operands "

6. Types Of Addressing Modes:

Various types of addressing modes are:

1. Implied and Immediate Addressing Modes

2. Direct or Indirect Addressing Modes
3. Register Addressing Modes
4. Register Indirect Addressing Mode
5. Auto-Increment and Auto-Decrement Addressing Modes
6. Displacement Based Addressing Modes

7. Implied Addressing Mode also known as "Implicit" or "Inherent" addressing mode is the addressing mode in which, no operand(register or memory location or data) is specified in the instruction. As in this mode the operand are specified implicit in the definition of instruction.

8. In Immediate Addressing Mode operand is specified in the instruction itself.In other words, an immediate mode instruction has an operand field rather than an address field, which contain actual operand to be used in conjunction with the operand specified in the instruction

9. Direct Addressing Mode is also known as “Absolute Addressing Mode”.In this mode the address of data(operand) is specified in the instruction itself.That is, in this type of mode, the operand resides in memory and its address is given directly by the address field of the instruction

10. In this mode, the address field of instruction gives the memory address where on, the operand is stored in memory.That is, in this mode, the address field of the instruction gives the address where the “Effective Address” is stored in memory.

11. In Register Addressing Mode, the operands are in registers that reside within the CPU.That is, in this mode, instruction specifies a register in CPU, which contain the operand.It is like Direct Addressing Mode, the only difference is that the address field refers to a register instead of memory location.

12. In Register Indirect Addressing Mode, the instruction specifies a register in CPU whose contents give the operand in memory.In other words, the selected register contain the address of operand rather than the operand itself

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14.

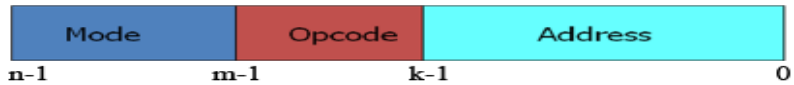

Fig: Instruction format with mode field

15. Instruction sets are differentiated by the following: • Number of bits per instruction. • Stack-based or register-based. • Number of explicit operands per instruction. • Operand location. • Types of operations. • Type and size of operands

16. Stack machines use one- and zero-operand instructions. • PUSH and POP instructions require a single memory address operand. • PUSH and POP operations involve only the stack's top element.

17. In stack addressing the operand is assumed to be on top of the stack.

18. Suppose a fetch-decode-execute cycle were broken into the following smaller steps: • Suppose we have a six-stage pipeline. S1 fetches the instruction, S2 decodes it, S3 determines the address of the operands, S4 fetches them, S5 executes the instruction, and S6 stores the result.

19. The **CISC** approach attempts to minimize the number of instructions per program, sacrificing the number of cycles per instruction. **Computers** based on the **CISC architecture** are designed to decrease the memory cost. ... **CISC** uses minimum possible instructions by implementing hardware and executes operations.

20. But Binary number system is most relevant and popular for representing **numbers** in digital **computer** system. Storing Real Number: ... In **fixed point** notation, there are a **fixed** number of digits after the decimal **point**, whereas floating **point** number allows for a varying number of digits after the decimal **point**

21. his representation does not reserve a specific number of bits for the integer part or the fractional part. Instead it reserves a certain number of bits for the number (called the mantissa or significand) and a certain number of bits to say where within that number the decimal place sits (called the exponent)

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I.SHORT ANSWER QUESTIONS[2M]

1. Perform $(-15)_{10} + (+3)_{10}$ using 2's compliment. [March 2017]
2. Discuss the metrics used in the performance of a computer. [March 2017]
3. Write down the differences between a microprocessor and micro controller.[March 2017]
4. Convert the 1998 (decimal number) to binary. [NOV 2015]
5. Describe about ***High-Impedance*** State. [NOV 2015]
6. A digital computer has a common bus system for 16 registers of 32 bits each. The bus is constructed with multiplexers. How many selection inputs are there in each multiplexer? [NOV /DEC 2016]

7 .Give one example for Arithmetic Micro Operations, Logic Micro Operations and Shift Micro Operations. [NOV /DEC 2016]

8.What is the difference between hardwired control and a micro programmed control? [NOV /DEC 2016]

9. With a neat diagram explain the basic operational concepts of computer. [NOV /DEC 2017]

10.What is Stack Organization? . [NOV /DEC 2017]

11. Define Cache Memory. . [NOV /DEC 2017]

12. What is a Micro Program? . [NOV /DEC 2017]

13.Draw and explain micro instruction format[May 2018]

14.classify Arithmetic micro operations. [May 2018]

II.LONG ANSWER QUESTIONS[5M]

1 a.How index addressing mode is different from relative addressing mode? Explain.

b.Obtain the 9's and 10's complement of the following six digit decimal numbers: 123901, 090567.[March 2017]

2) Draw the block diagram of a 4-bit parallel adder and subtractor and explain its significance and functionality. [March 2017]

3. Describe about shift micro operations.[NOV 2015]

b) Obtain the 2's complement of following eight bits numbers

i) 1010110

ii) 10000001 [NOV 2015]

4. Convert the hexadecimal number F3A7C2 to binary and octaL[NOV 2015]

5. Explain in detail about 4-bit Arithmetic circuit. [NOV 2015]

6.Describe about Arithmetic Logic Shift Unit. [NOV 2015]

7. Explain how floating point numbers are represented[NOV /DEC 2016]

8. What is an Addressing mode? List and explain the various addressing modes with an example. [NOV /DEC 2016]

9. Design a 4 bit combinational circuit decrement using four full adder circuits. [NOV /DEC 2016]

10. Explain with an example Booth's algorithm for multiplication of signed 2's complement numbers. [NOV /DEC 2016]

11. With a neat block diagram, explain in detail about micro programmed control unit and explain its operations. [NOV /DEC 2016]

12. Explain about different modes of transfer. [NOV /DEC 2017]

13. Explain the instruction cycle with a neat flow chart. [NOV /DEC 2017]

14 Give explanation about the fixed point and floating point representations in detail. [NOV /DEC 2017]

15. calculate arithmetic operations(+70)+(+80)and (-70)+(-80) with binary numbers in Signed 2's complement representation.use eight bits to accommodate each number together with sign.show that overflow occurs in both cases[May 2018]
16.Expalin different shift Micro-operations with Examples. [May 2018]
17.Explain binary adder subtractor in detail. [May 2018]

CHOOSE THE CORRECT ANSWER

1. Which operations are used for addition, subtraction, increment, decrement and complement function:

a. Bus
b. Memory transfer
c. Arithmetic operation
d. All of t

2.The length of a register is called _____ (b)
a) word limit
b) word size
c) register limit
d) register size

3.Which of the following is not a visible register? (d)
a) General Purpose Registers
b) Address Register
c) Status Register
d) MAR

4.The number of sign bits in a 32-bit IEEE format _____(a)
a) 1
b) 11
c) 9
d) 23

5.The sign magnitude representation of -1 is _____(d)
a) 0001
b) 1110
c) 1000
d) 1001

6.The maximum number of bits sufficient to represent a hexadecimal number in binary: (a)
a) 4
b) 3
c) 7
d) 8

7.Convert $(6532)_8$ to hexadecimal. c
a) A01
b) A02
c) B01
d) C01

8. The instruction, Add Loc,R1 in RTN is ____(d)
a) AddSetCC Loc+R1
b) R1=Loc+R1

c) Not possible to write in RTN
d) R1<-[Loc]+[R1]
9.In a system, which has 32 registers the register id is _____ long.(C)
a) 16 bit
b) 8 bits
c) 5 bits
d) 6 bits
10.When generating physical addresses from a logical address the offset is stored in _____(b)
a) Translation look-aside buffer
b) Relocation register
c) Page table
d) Shift register
11.Which method/s of representation of numbers occupies a large amount of memory than others? (A)
a) Sign-magnitude
b) 1's complement
c) 2's complement
d) 1's & 2's compliment
12.When we perform subtraction on -7 and 1 the answer in 2's complement form is _____(d)
a) 1010
b) 1110
c) 0110
d) 1000
13.In some pipelined systems, a different instruction is used to add to numbers which can affect the flags upon execution. That instruction is _____(a)
a) AddSetCC
b) AddCC
c) Add++
d) SumSetCC
14.For the addition of large integers, most of the systems make use of _____(c)
a) Fast adders
b) Full adders
c) Carry look-ahead adders
d) None of the mentioned
15.The sign followed by the string of digits is called as _____(c)
a) Significant
b) Determinant
c) Mantissa
d) Exponent
16.The normalized representation of $0.0010110 * 2_9$ is _____(b)
a) 0 10001000 0010110
b) 0 10000101 0110
c) 0 10101010 1110
d) 0 11110100 11100
17. The main virtue for using single Bus structure is _____(c)
a) Fast data transfers

b) Cost effective connectivity and speed
c) Cost effective connectivity and ease of attaching peripheral devices
d) None of the mentioned
18. The bus used to connect the monitor to the CPU is _____(b)
a) PCI bus
b) SCSI bus
c) Memory bus
d) Rambus
19. The special memory used to store the micro routines of a computer is _____(b)
a) Control table
b) Control store
c) Control mart
d) Control shop
20.Every time a new instruction is loaded into IR the output of _____ is loaded into UPC.
a) Starting address generator
b) Loader
c) Linker
d) Clock
Anwer (a)

UNIT 2 MICRO PROGRAMMED CONTROL AND HARDWIRED UNIT IMPORTANT POINTS

1.A control unit whose binary control variables are stored in memory is called a micro programmed control unit.
2.In computer central processing units, micro-operations (also known as a micro-ops or μops) are detailed low-level instructions used in some designs to implement complex machine instructions (sometimes termed macro-instructions in this context)
3. Since alterations of the microprogram are not needed once the control unit is in operation, the control memory can be a read-only memory (ROM).
4. Microinstructions can be saved by employing subroutines that use common sections of microcode
5. The control memory address register specifies the address of the microinstruction, and the control data register holds the microinstruction read from memory.
6. The microinstruction contains a control word that specifies one or more microoperations for the data processor. Once these operations are executed, the control must determine the next address.
7.The location of the next microinstruction may be the one next in sequence, or it may be located somewhere else in the control memory
8. The basic components of a microprogrammed control unit are the control memory and the circuits that select the next address. The address selection part is called a microprogram sequencer. A microprogram sequencer can be constructed with digital functions to suit a particular application.
9. Each step in a sequence of steps in the execution of a certain machine instruction is considered as a *microinstruction*, and it is represented by a control word. All of the bits corresponding to the control signals that need to be asserted in this step are set to 1, and all others are set to 0
10. The microroutines for all instruction in the instruction set of a computer are stored in a special memory called the control memory (CM)
11. **Control Buffer Register(CBR):**When microinstruction is read from the control memory, it is transferred to a control Buffer Register (CBR), which is similar to the instruction Register (IR) that stores the opcode of the instruction read from the memory.

SHORT ANSWER QUESTIONS:

1.Give a brief note on PROM.[MARCH 2017]
2. Mention the basic differences between an Isolated I/O and Memory-Mapped I/O[MARCH 2017]
3.Define Control Memory. [NOV 2015]
4.Write about Control Function. [NOV 2015]
5. What is the difference between hardwired control and a micro programmed control? [DEC 2016]
6. Differentiate between SRAM and DRAM. [DEC 2016]
7.Define Cache Memory. . [NOV 2017]
8.What is a Micro Program? . [NOV 2017]
9.Draw and explain Micro Instruction format? [May 2018]
10.Explain about virtual memory?[may 2018]

LONG ANSWER QUESTIONS:

1. With the help of a neat block diagram, explain the decision-making capabilities in the control unit. [MARCH 2017]
2. Explain the cache memory mapping techniques with relevant diagrams. [MARCH 2017]
3. Describe about shift micro operations. [NOV 2015]
4. Explain in detail about RAID structure. [NOV 2015][DEC 2016]
5. With a neat block diagram, explain in detail about micro programmed control unit and explain its operations[DEC 2016]

[or]

6. Explain organization of microprogmmed control unit in detail?
7. A block set associative cache consists of a total of 64 blocks divided into 4 blocks sets. The main memory contains 4096 blocks, each consisting of 128 words. [DEC 2016]
   i) How many bits are there in main memory address?
   ii) How many bits are there in each of the TAG, SET, and WORD fields?
8. a.In What situations would use memory as a RAM disk be more useful than using it as a disk cache?
   b) Give a brief note on free space management. [DEC 2016]
9. What is Virtual Memory? Explain in detail. [NOV 2017]
10. With neat diagram, explain address selection for control memory. [NOV 2017]
11. What are the goals of memory management? Explain the Contiguous Memory Allocation t echniques. [NOV 2017]
12. Explain organization of Kx1 memory chip with neat diagram?[May 2018]

13. explain Associative mapping technique with its advantages and disadvantages? [May 2018]

CHOOSE THE CORRECT ANSWER

1. In micro-programmed approach, the signals are generated by _____(A)
a) Machine instructions
b) System programs
c) Utility tools
d) None of the mentioned
2. Individual control words of the micro routine are called as _____(C)
a) Micro task
b) Micro operation
c) Micro instruction
d) Micro command
3. Every time a new instruction is loaded into IR the output of _____ is loaded into UPC. (A)
a) Starting address generator
b) Loader
c) Linker
d) Clock
4. A word whose individual bits represent a control signal is _____(B)
a) Command word
b) Control word
c) Co-ordination word
d) Generation word

5. To read the control words sequentially _____ is used. (C)
a) PC
b) IR
c) UPC
d) None of the mentioned
6. The data is transferred over the RAMBUS as _____(C)
a) Packets
b) Blocks
c) Swing voltages
d) Bits
7. The type of signaling used in RAMBUS is _____(B)
a) CLK signaling
b) Differential signaling
c) Integral signaling
d) None of the mentioned
8. The PROM is more effective than ROM chips in regard to _____(D)
a) Cost
b) Memory management
c) Speed of operation
d) Both Cost and Speed of operation
9. The difference between the EPROM and ROM circuitry is _____(C)
a) The usage of MOSFET's over transistors
b) The usage of JFET's over transistors
c) The usage of an extra transistor
d) None of the mentioned
10. The disadvantage of the EPROM chip is _____(D)
a) The high cost factor
b) The low efficiency
c) The low speed of operation
d) The need to remove the chip physically to reprogram it
11. The memory devices which are similar to EEPROM but differ in the cost effectiveness is _____(C)
a) Memory sticks
b) Blue-ray devices
c) Flash memory
d) CMOS
12. The binary address issued to data or instructions are called as _____(D)
a) Physical address
b) Location
c) Relocatable address
d) Logical address
13. The main aim of virtual memory organisation is _____(D)
a) To provide effective memory access
b) To provide better memory transfer
c) To improve the execution of the program
d) All of the mentioned
14. The main purpose of having memory hierarchy is to _____(D)
a) Reduce access time

b) Provide large capacity
c) Reduce propagation time
d) Reduce access time & Provide large capacity

15. An effective to introduce parallelism in memory access is by _____(A)
a) Memory interleaving
b) TLB
c) Pages
d) Frames

16. The minimum time delay between two successive memory read operations is _____(A)
a) Cycle time
b) Latency
c) Delay
d) None of the mentioned

17. _____ is the bottleneck, when it comes computer performance. (B)
a) Memory access time
b) Memory cycle time
c) Delay
d) Latency

18. The drawback of building a large memory with DRAM is _____(C)
a) The large cost factor
b) The inefficient memory organisation
c) The Slow speed of operation
d) All of the mentioned

19. The effectiveness of the cache memory is based on the property of _____(A)
a) Locality of reference
b) Memory localisation
c) Memory size
d) None of the mentioned

20. The write-through procedure is used _____ (C)
a) To write onto the memory directly
b) To write and read from memory simultaneously
c) To write directly on the memory and the cache simultaneously
d) None of the mentioned